# Table of contents provided by Syndetics


- **Faults in Digital Circuits: Failures and Faults**
- **Modeling of Faults**
- **Temporary Faults**
- **Test Generation for Combinational Logic Circuits: Fault Diagnosis of Digital Circuits**
- **Test Generation Techniques for Combinatorial Circuits**
- **Multiple Fault Detection in Combinational Logic Circuits**
- **Testable Combinational Logic Circuit Design: The Reed-Muller Expansion Technique**
- **Three Level OR-AND-OR Design**
- **Automatic Synthesis of Testable Logic**
- **Testable Design of Multi-Level Combinational Circuits**
- **Synthesis of Random Pattern Testable Combinational Circuits**
- **Path Delay Fault Testable Combinational Logic Design**
- **Testable PLA Design**
- **Test Generation for Sequential Circuits: Testing of Sequential Circuits as IterativeCombinational Circuits**
- **State Table Verification**
- **Test Generation Based on Circuit Structure**
- **Functional Fault Models**
- **Test Generation Based on Functional Fault Models**
- **Design of Testable Sequential Circuits: Controllability and Observability**
- **Ad hoc Design Rules for Improving Testability**
- **Design of Diagnosable Sequential Circuits**
- **The Scan-Path Technique for Testable Sequential Circuit Design**
- **Level-Sensitive Scan Design (LSSD**
- **Random Access Scan Technique**
- **Partial Scan**
- **Testable Sequential Circuit Design Using Non-Scan Techniques**
- **Cross Check**
- **Boundary Scan**
- **Built-In Self Test: Test Pattern for BIST**
- **Output Response Analysis**
- **Circular BIST**
- **BIST Architecture**
- **Testable Memory Design: RAM Fault Models**
- **Test Algorithms for RAMs**
- **Detection of Pattern Sensitive Faults**
- **BIST Techniques for RAM Chips**
- **Test Generation and BIST for Embedded RAMs**
- **Subject Index**