Table of contents provided by Syndetics

- **Chapter 1 Models for Integrated-Circuit Active Devices** (p. 1)
- **1.1 Introduction** (p. 1)
- **1.2 Depletion Region of a pn Junction** (p. 1)
- **1.3 Large-Signal Behavior of Bipolar Transistors** (p. 8)
- **1.4 Small-Signal Models of Bipolar Transistors** (p. 26)
- **1.5 Large Signal Behavior of Metal-Oxide-Semiconductor Field-Effect Transistors** (p. 38)
- **1.6 Small-Signal Models of the MOS Transistors** (p. 49)
- **1.7 Short-Channel Effects in MOS Transistors** (p. 58)
- **1.8 Weak Inversion in MOS Transistors** (p. 65)
- **1.9 Substrate Current Flow in MOS Transistors** (p. 71)
- **A.1.1 Summary of Active-Device Parameters** (p. 73)
- **Chapter 2 Bipolar, MOS, and BiCMOS Integrated-Circuit Technology** (p. 78)
- **2.1 Introduction** (p. 78)
- **2.2 Basic Processes in Integrated-Circuit Fabrication** (p. 79)
- **2.3 High-Voltage Bipolar Integrated-Circuit Fabrication** (p. 88)
- **2.4 Advanced Bipolar Integrated-Circuit Fabrication** (p. 92)
- **2.5 Active Devices in Bipolar Analog Integrated Circuits** (p. 95)
- **2.6 Passive Components in Bipolar Integrated Circuits** (p. 115)
- **2.7 Modifications to the Basic Bipolar Process** (p. 123)
- **2.8 MOS Integrated-Circuit Fabrication** (p. 127)
- **2.9 Active Devices in MOS Integrated Circuits** (p. 131)
- **2.10 Passive Components in MOS Technology** (p. 144)
- **2.11 BiCMOS Technology** (p. 150)
- **2.12 Heterojunction Bipolar Transistors** (p. 152)
- **2.13 Interconnect Delay** (p. 153)
- **2.14 Economics of Integrated-Circuit Fabrication** (p. 154)
- **2.15 Packaging Considerations for Integrated Circuits** (p. 159)
- **A.2.1 SPICE Model-Parameter Files** (p. 163)
- **Chapter 3 Single-Transistor and Multiple-Transistor Amplifiers** (p. 170)
- **3.1 Device Model Selection for Approximate Analysis of Analog Circuits** (p. 171)
- **3.2 Two-Port Modeling of Amplifiers** (p. 172)
- **3.3 Basic Single-Transistor Amplifier Stages** (p. 174)
- **3.4 Multiple-Transistor Amplifier Stages** (p. 202)
- **3.5 Differential Pairs** (p. 215)
- **A.3.1 Elementary Statistics and the Gaussian Distribution** (p. 246)
- **Chapter 4 Current Mirrors, Active Loads, and References** (p. 253)
- **4.1 Introduction** (p. 253)
- **4.2 Current Mirrors** (p. 253)
- **4.3 Active Loads** (p. 278)
- **4.4 Voltage and Current References** (p. 299)
- **A.4.1 Matching Considerations in Current Mirrors** (p. 327)
- **A.4.2 Input Offset Voltage of Differential Pair with Active Load** (p. 332)
- **Chapter 5 Output Stages** (p. 344)

- **5.1 Introduction** (p. 344)
- **5.2 The Emitter Follower As an Output Stage** (p. 344)
- **5.3 The Source Follower As an Output Stage** (p. 356)
- **5.4 Class B Push-Pull Output Stage** (p. 362)
- **5.5 CMOS Class AB Output Stages** (p. 382)
- **Chapter 6 Operational Amplifiers with Single-Ended Outputs** (p. 404)
- **6.1 Applications of Operational Amplifiers** (p. 405)
- **6.2 Deviations from Ideality in Real Operational Amplifiers** (p. 419)
- **6.3 Basic Two-Stage MOS Operational Amplifiers** (p. 425)
- **6.4 Two-Stage MOS Operational Amplifiers with Cascodes** (p. 442)
- **6.5 MOS Telescopic-Cascode Operational Amplifiers** (p. 444)
- **6.6 MOS Folded-Cascode Operational Amplifiers** (p. 446)
- **6.7 MOS Active-Cascode Operational Amplifiers** (p. 450)
- **6.8 Bipolar Operational Amplifiers** (p. 453)
- **6.9 Design Considerations for Bipolar Monolithic Operational Amplifiers** (p. 472)
- **Chapter 7 Frequency Response of Integrated Circuits** (p. 488)
- **7.1 Introduction** (p. 488)
- **7.2 Single-Stage Amplifiers** (p. 488)
- **7.3 Multistage Amplifier Frequency Response** (p. 516)
- **7.4 Analysis of the Frequency Response of the 741 Op Amp** (p. 537)
- **7.5 Relation Between Frequency Response and Time Response** (p. 542)
- **Chapter 8 Feedback** (p. 553)
- **8.1 Ideal Feedback Equation** (p. 553)
- **8.2 Gain Sensitivity** (p. 555)
- **8.3 Effect of Negative Feedback on Distortion** (p. 555)
- **8.4 Feedback Configurations** (p. 557)
- **8.5 Practical Configurations and the Effect of Loading** (p. 563)
- **8.6 Single-Stage Feedback** (p. 587)
- **8.7 The Voltage Regulator as a Feedback Circuit** (p. 593)
- **8.8 Feedback Circuit Analysis Using Return Ratio** (p. 599)
- **9.2 Relation Between Gain and Bandwidth in Feedback Amplifiers** (p. 624)
- **8.9 Modeling Input and Output Ports in Feedback Circuits** (p. 613)
- **Chapter 9 Frequency Response and Stability of Feedback Amplifiers** (p. 624)
- **9.1 Introduction** (p. 624)
- **9.3 Instability and the Nyquist Criterion** (p. 626)
- **9.4 Compensation** (p. 633)
- **9.5 Root-Locus Techniques** (p. 664)
- **9.6 Slew Rate** (p. 680)
- **A.9.1 Analysis in Terms of Return-Ratio Parameters** (p. 691)
- **A.9.2 Roots of a Quadratic Equation** (p. 692)
- **Chapter 10 Nonlinear Analog Circuits** (p. 702)
- **10.1 Introduction** (p. 702)
- **10.2 Precision Rectification** (p. 702)
- **10.3 Analog Multipliers Employing the Bipolar Transistor** (p. 708)
- **10.4 Phase-Locked Loops (PLL)** (p. 720)
- **10.5 Nonlinear Function Symbols** (p. 743)

- **Chapter 11 Noise in Integrated Circuits** (p. 748)
- **11.1 Introduction** (p. 748)
- **11.2 Sources of Noise** (p. 748)
- **11.3 Noise Models of Integrated-Circuit Components** (p. 756)
- **11.4 Circuit Noise Calculations** (p. 760)
- **11.5 Equivalent Input Noise Generators** (p. 768)
- **11.6 Effect of Feedback on Noise Performance** (p. 776)
- **11.7 Noise Performance of Other Transistor Configurations** (p. 783)
- **11.8 Noise in Operational Amplifiers** (p. 788)
- **11.9 Noise Bandwidth** (p. 794)
- **11.10 Noise Figure and Noise Temperature** (p. 799)
- **Chapter 12 Fully Differential Operational Amplifiers** (p. 808)
- **12.1 Introduction** (p. 808)
- **12.2 Properties of Fully Differential Amplifiers** (p. 808)
- **12.6 Fully Differential Op Amps** (p. 835)
- **12.3 Small-Signal Models for Balanced Differential Amplifiers** (p. 811)
- **12.4 Common-Mode Feedback** (p. 816)
- **12.5 CMFB Circuits** (p. 823)
- **12.7 Unbalanced Fully Differential Circuits** (p. 850)
- **12.8 Bandwidth of the CMFB Loop** (p. 856)
- **Index** (p. 865)