- Preface p. xvii
- 1 Introduction p. 1
- 1.1 Introduction p. 1
- 1.2 Quality p. 2
- 1.3 The Test p. 2
- 1.4 The Design Process p. 6
- 1.5 Design Automation p. 9
- 1.6 Estimating Yield p. 11
- 1.7 Measuring Test Effectiveness p. 14
- 1.8 The Economics of Test p. 20
- 1.9 Case Studies p. 23
- 1.10 Summary p. 26
- Problems p. 29
- References p. 30
- 2 Simulation p. 33
- 2.1 Introduction p. 33
- 2.2 Background p. 33
- 2.3 The Simulation Hierarchy p. 36
- 2.4 The Logic Symbols p. 37
- 2.5 Sequential Circuit Behavior p. 39
- 2.6 The Compiled Simulator p. 44
- 2.7 Event-Driven Simulation p. 54
- 2.8 Multiple-Valued Simulation p. 61
- 2.9 Implementing the Nominal-Delay Simulator p. 64
- 2.10 Switch-Level Simulation p. 74
- 2.11 Binary Decision Diagrams p. 86
- 2.12 Cycle Simulation p. 101
- 2.13 Timing Verification p. 106
- 2.14 Summary p. 110
- Problems p. 111
- References p. 116
- 3 Fault Simulation p. 119
- 3.1 Introduction p. 119
- 3.2 Approaches to Testing p. 120
- 3.3 Analysis of a Faulted Circuit p. 122
- 3.4 The Stuck-At Fault Model p. 125
- 3.5 The Fault Simulator: An Overview p. 131
- 3.6 Parallel Fault Processing p. 134
- 3.7 Concurrent Fault Simulation p. 139
- 3.8 Delay Fault Simulation p. 147
- 3.9 Differential Fault Simulation p. 149
- 3.10 Deductive Fault Simulation p. 151
- 3.11 Statistical Fault Analysis p. 152
- 3.12 Fault Simulation Performance p. 155
- 3.13 Summary p. 157
- Problems p. 159

- References p. 162
- 4 Automatic Test Pattern Generation p. 165
- 4.1 Introduction p. 165
- 4.2 The Sensitized Path p. 165
- 4.3 The D-Algorithm p. 170
- 4.4 Testdetect p. 182
- 4.5 The Subscripted D-Algorithm p. 184
- 4.6 PODEM p. 188
- 4.7 FAN p. 193
- 4.8 Socrates p. 202
- 4.9 The Critical Path p. 205
- 4.10 Critical Path Tracing p. 208
- 4.11 Boolean Differences p. 210
- 4.12 Boolean Satisfiability p. 216
- 4.13 Using BDDs for ATPG p. 219
- 4.14 Summary p. 224
- Problems p. 226
- References p. 230
- 5 Sequential Logic Test p. 233
- 5.1 Introduction p. 233
- 5.2 Test Problems Caused by Sequential Logic p. 233
- 5.3 Sequential Test Methods p. 239
- 5.4 Sequential Logic Test Complexity p. 259
- 5.5 Experiments with Sequential Machines p. 266
- 5.6 A Theoretical Limit on Sequential Testability p. 272
- 5.7 Summary p. 277
- Problems p. 278
- References p. 280
- 6 Automatic Test Equipment p. 283
- 6.1 Introduction p. 283
- 6.2 Basic Tester Architectures p. 284
- 6.3 The Standard Test Interface Language p. 288
- 6.4 Using the Tester p. 293
- 6.5 The Electron Beam Probe p. 299
- 6.6 Manufacturing Test p. 301
- 6.7 Developing a Board Test Strategy p. 304
- 6.8 The In-Circuit Tester p. 307
- 6.9 The PCB Tester p. 310
- 6.10 The Test Plan p. 315
- 6.11 Visual Inspection p. 316
- 6.12 Test Cost p. 319
- 6.13 Summary p. 319
- Problems p. 320
- References p. 321
- 7 Developing a Test Strategy p. 323
- 7.1 Introduction p. 323

- 7.2 The Test Triad p. 323
- 7.3 Overview of the Design and Test Process p. 325
- 7.4 A Testbench p. 327
- 7.5 Fault Modeling p. 331
- 7.6 Technology-Related Faults p. 337
- 7.7 The Fault Simulator p. 341
- 7.8 Behavioral Fault Modeling p. 353
- 7.9 The Test Pattern Generator p. 368
- 7.10 Miscellaneous Considerations p. 378
- 7.11 Summary p. 382
- Problems p. 383
- References p. 385
- 8 Design-For-Testability p. 387
- 8.1 Introduction p. 387
- 8.2 Ad Hoc Design-for-Testability Rules p. 388
- 8.3 Controllability/Observability Analysis p. 396
- 8.4 The Scan Path p. 407
- 8.5 The Partial Scan Path p. 426
- 8.6 Scan Solutions for PCBs p. 432
- 8.7 Summary p. 443
- Problems p. 444
- References p. 449
- 9 Built-In Self-Test p. 451
- 9.1 Introduction p. 451
- 9.2 Benefits of BIST p. 452
- 9.3 The Basic Self-Test Paradigm p. 454
- 9.4 Random Pattern Effectiveness p. 464
- 9.5 Self-Test Applications p. 471
- 9.6 Remote Test p. 484
- 9.7 Black-Box Testing p. 488
- 9.8 Fault Tolerance p. 495
- 9.9 Summary p. 505
- Problems p. 507
- References p. 510
- 10 Memory Test p. 513
- 10.1 Introduction p. 513
- 10.2 Semiconductor Memory Organization p. 514
- 10.3 Memory Test Patterns p. 517
- 10.4 Memory Faults p. 521
- 10.5 Memory Self-Test p. 524
- 10.6 Repairable Memories p. 535
- 10.7 Error Correcting Codes p. 537
- 10.8 Summary p. 546
- Problems p. 547
- References p. 549
- 11 I[subscript DDQ] p. 551

- 11.1 Introduction p. 551
- 11.2 Background p. 551
- 11.3 Selecting Vectors p. 553
- 11.4 Choosing a Threshold p. 556
- 11.5 Measuring Current p. 557
- 11.6 I[subscript DDQ] Versus Burn-In p. 559
- 11.7 Problems with Large Circuits p. 562
- 11.8 Summary p. 564
- Problems p. 565
- References p. 565
- 12 Behavioral Test and Verification p. 567
- 12.1 Introduction p. 567
- 12.2 Design Verification: An Overview p. 568
- 12.3 Simulation p. 570
- 12.4 Measuring Simulation Thoroughness p. 575
- 12.5 Random Stimulus Generation p. 581
- 12.6 The Behavioral ATPG p. 587
- 12.7 The Sequential Circuit Test Search System (SCIRTSS) p. 597
- 12.8 The Test Design Expert p. 607
- 12.9 Design Verification p. 635
- 12.10 Summary p. 650
- Problems p. 652
- References p. 653
- Index p. 657