

- Preface p. ix
- 1 Basic Principles of Digital Systems p. 1
- 1.1 Digital Versus Analog Electronics p. 2
- 1.2 Digital Logic Levels p. 3
- 1.3 The Binary Number System p. 4
- 1.4 Hexadecimal Numbers p. 12
- 1.5 Digital Waveforms p. 15
- 2 Logic Functions and Gates p. 25
- 2.1 Basic Logic Functions p. 26
- 2.2 Logic Switches and LED Indicators p. 31
- 2.3 Derived Logic Functions p. 34
- 2.4 DeMorgan's Theorems and Gate Equivalence p. 37
- 2.5 Enable and Inhibit Properties of Logic Gates p. 41
- 2.6 Integrated Circuit Logic Gates p. 46
- 3 Boolean Algebra and Combinational Logic p. 57
- 3.1 Boolean Expressions, Logic Diagrams and Truth Tables p. 58
- 3.2 Sum-of-Products (SOP) and Product-of-Sums (POS) Forms p. 67
- 3.3 Theorems of Boolean Algebra p. 73
- 3.4 Simplifying SOP and POS Expressions p. 86
- 3.5 Simplification by the Karnaugh Map Method p. 90
- 4 Introduction to PLDs and MAX+PLUS II p. 115
- 4.1 What is a PLD? p. 116
- 4.2 Programming PLDs using MAX+PLUS II p. 118
- 4.3 Graphic Design File p. 120
- 4.4 Compiling MAX+PLUS II Files p. 127
- 4.5 Hierarchical Design p. 129
- 4.6 Text Design File (VHDL) p. 133
- 4.7 Creating a Physical Design p. 140
- 5 Combinational Logic Functions p. 155
- 5.1 Decoders p. 156
- 5.2 Encoders p. 179
- 5.3 Multiplexers p. 185
- 5.4 Demultiplexers p. 197
- 5.5 Magnitude Comparators p. 203
- 5.6 Parity Generators and Checkers p. 208
- 6 Digital Arithmetic and Arithmetic Circuits p. 221
- 6.1 Digital Arithmetic p. 222
- 6.2 Representing Signed Binary Numbers p. 225
- 6.3 Signed Binary Arithmetic p. 227
- 6.4 Hexadecimal Arithmetic p. 232
- 6.5 Numeric and Alphanumeric Codes p. 235
- 6.6 Binary Adders and Subtractors p. 239
- 6.7 BCD Adders p. 259
- 6.8 Carry Generation in MAX+PLUS II p. 263
- 7 Introduction to Sequential Logic p. 275
- 7.1 Latches p. 276

- 7.2 NAND/NOR Latches p. 279
- 7.3 Gated Latches p. 289
- 7.4 Edge-Triggered D Flip-Flops p. 298
- 7.5 Edge-Triggered JK Flip-Flops p. 303
- 7.6 Edge-Triggered T Flip-Flops p. 310
- 7.7 Timing Parameters p. 312
- 8 Introduction to Programmable Logic Architectures p. 329
- 8.1 Programmable Sum-of-Products Arrays p. 330
- 8.2 PAL Fuse Matrix and Combinational Outputs p. 332
- 8.3 PAL Outputs with Programmable Polarity p. 336
- 8.4 PAL Devices with Registered Outputs p. 341
- 8.5 Universal PAL and Generic Array Logic p. 345
- 8.6 MAX7000S CPLD p. 351
- 8.7 FLEX10K CPLD p. 354
- 9 Counters and Shift Registers p. 363
- 9.1 Basic Concepts of Digital Counters p. 364
- 9.2 Synchronous Counters p. 369
- 9.3 Design of Synchronous Counters p. 376
- 9.4 Programming Binary Counters in VHDL p. 385
- 9.5 Control Options for Synchronous Counters p. 388
- 9.6 Programming Presetable and Bidirectional Counters in VHDL p. 403
- 9.7 Shift Registers p. 413
- 9.8 Programming Shift Registers in VHDL p. 426
- 9.9 Shift Register Counters p. 438
- 10 State Machine Design p. 457
- 10.1 State Machines p. 457
- 10.2 State Machines With No Control Inputs p. 459
- 10.3 State Machines With Control Inputs p. 466
- 10.4 Switch Debouncer for a Normally Open Pushbutton Switch p. 475
- 10.5 Unused States in State Machines p. 484
- 10.6 Traffic Light Controller p. 490
- 11 Logic Gate Circuitry p. 497
- 11.1 Electrical Characteristics of Logic Gates p. 498
- 11.2 Propagation Delay p. 502
- 11.3 Fanout p. 505
- 11.4 Power Dissipation p. 510
- 11.5 Noise Margin p. 514
- 11.6 Interfacing TTL and CMOS Gates p. 516
- 11.7 Internal Circuitry of TTL gates p. 518
- 11.8 Internal Circuitry of CMOS Gates p. 540
- 11.9 TTL and CMOS Variations p. 551
- 12 Interfacing Analog and Digital Circuitry p. 565
- 12.1 Analog and Digital Signals p. 566
- 12.2 Digital-to-Analog Conversion p. 571
- 12.3 Analog-to-Digital Conversion p. 591
- 12.4 Data Acquisition p. 605

- 13 Memory Devices and Systems p. 621
- 13.1 Basic Memory Concepts p. 622
- 13.2 Random Access Read/Write Memory (RAM) p. 630
- 13.3 Read Only Memory (ROM) p. 636
- 13.4 Sequential Memory: FIFO and LIFO p. 645
- 13.5 Dynamic RAM Modules p. 646
- 13.6 Memory Systems p. 648
- Appendix A Altera UP-1 User's Guide p. 657
- Appendix B VHDL Language Reference p. 689
- Appendix C Data Sheets p. 702
- Appendix D CMOS Handling Precautions p. 766
- Appendix E EPROM/ROM Data for a Digital Function Generator p. 768
- Answers to Selected Odd-Numbered Problems p. 775
- Index p. 839