- Preface p. ix
- Chapter 1 Introduction to Digital Concepts p. 1
- Activity 1.1 The Concept of a Digital Circuit p. 2
- Activity 1.2 Binary Digits and Logic Levels p. 3
- Activity 1.3 Boolean Algebra--AND, OR, and NOT Functions p. 4
- Activity 1.4 Troubleshooting Problems p. 6
- Activity 1.5 Circuit Construction p. 7
- Chapter 2 Logic Gates and Combinational Circuits p. 9
- Activity 2.1 The Inverter or NOT Gate p. 9
- Activity 2.2 The OR Gate p. 14
- Activity 2.3 The AND Gate p. 18
- Activity 2.4 The NAND Gate p. 22
- Activity 2.5 The NOR Gate p. 28
- Activity 2.6 The Buffer Gate p. 34
- Chapter 3 Advanced Logic Gates p. 36
- Activity 3.1 The Exclusive OR (XOR) Gate p. 36
- Activity 3.2 The Exclusive NOR (XNOR) Gate p. 39
- Activity 3.3 The NAND as a Universal Gate p. 42
- Activity 3.4 The NOR as a Universal Gate p. 49
- Activity 3.5 Working With Boolean Formulas and Combinational Circuits p. 53
- Chapter 4 Arithmetic Circuits p. 57
- Activity 4.1 Adder Circuits p. 58
- Activity 4.2 1's (One's) Complement Subtractor Circuits p. 61
- Activity 4.3 Looking at the 2's (Two's) Complement Subtractor Circuit/Method p. 62
- Chapter 5 Open Collector Gates and Tri-State Circuits p. 64
- Activity 5.1 Open Collector Outputs p. 65
- Activity 5.2 Tri-State Circuits p. 68
- Chapter 6 Sequential Circuits: NAND/NOR Latches p. 72
- Activity 6.1 The SET-RESET (S-R) Latch Circuit (Crossed-NAND) p. 73
- Activity 6.2 The SET-RESET (S-R) Latch Circuit (Crossed-NOR) p. 75
- Activity 6.3 Using an S-R Latch Circuit to Debounce a Switch p. 77
- Activity 6.4 The Gated S-R Latch Circuit p. 78
- Activity 6.5 The Gated D (Transparent) Latch Circuit p. 80
- Activity 6.6 The 74LS75N Quad S-R Latch IC p. 82
- Activity 6.7 Using the 4043BD Quad (CMOS) S-R Latch IC p. 84
- Chapter 7 Sequential Circuits: Flip-Flops p. 86
- Activity 7.1 The Logic of an Edge-Triggering Circuit p. 86
- Activity 7.2 The Edge-Triggered D Flip-Flop p. 87
- Activity 7.3 The Edge-Triggered J-K Flip-Flop p. 89
- Activity 7.4 Toggle (Trigger) Flip-Flops p. 93
- Chapter 8 Sequential Circuits: Counters p. 96
- Activity 8.1 The Asynchronous (Ripple) Counter p. 97
- Activity 8.2 The Synchronous Counter p. 102
- Activity 8.3 Synchronous Down and Up/Down Counters p. 105

- Activity 8.4 Pre-settable Counters p. 109
- Chapter 9 Sequential Circuits: Shift Registers p. 113
- Activity 9.1 Serial In/Serial Out Shift Registers p. 115
- Activity 9.2 Serial In/Parallel Out Shift Registers p. 119
- Activity 9.3 Parallel In/Serial Out Shift Registers p. 122
- Activity 9.4 Parallel In/Parallel Out Shift Registers p. 127
- Chapter 10 Schmitt Trigger, One-Shot and Clock Circuits p. 132
- Activity 10.1 Schmitt Trigger Circuits for Wave Shaping and Clocks p. 132
- Activity 10.2 The 555 Integrated Circuit as an Astable Multivibrator p. 136
- Activity 10.3 The 555 Integrated Circuit as a Monostable Multivibrator p. 138
- Activity 10.4 One-Shot Circuits p. 140
- Activity 10.5 Crystal Oscillator Clock Circuits p. 142
- Chapter 11 Digital-to-Analog and Analog-to-Digital Converter Circuits p. 144
- Activity 11.1 Digital-to-Analog Conversion: Voltage Output p. 145
- Activity 11.2 Digital-to-Analog Conversion: Current Output p. 148
- Activity 11.3 Analog-to-Digital Conversion p. 152
- Chapter 12 Decoders, Encoders, Code Converters, and Displays p. 155
- Activity 12.1 Binary-to-Decimal Decoder Circuits p. 156
- Activity 12.2 BCD-to-Decimal Decoder Circuits p. 158
- Activity 12.3 BCD-to-Seven-Segment Decoder/Driver Circuits and Seven-Segment Displays p. 160
- Activity 12.4 Displaying Hexadecimal Numbers With Decoded Seven-Segment Displays p.
 163
- Activity 12.5 Encoding--Decimal to BCD (Ten-to-Four-Line) p. 166
- Chapter 13 More Combinational Circuits: Multiplexers and Demultiplexers p. 169
- Activity 13.1 Multiplexing Digital Data p. 170
- Activity 13.2 Demultiplexing Digital Data p. 173