- Section I Fabrication and Technology
- 1 Trends and Projections for the Future of Scaling and Future Integration Trends Hiroshi Iwai and Shun-ichiro Ohmi p. 1
- 2 CMOS Circuits
- 2.1 VLSI Circuits Eugene John p. 1
- 2.1 Pass-Transistor CMOS Circuits Shunzo Yamashita p. 20
- 2.1 Synthesis of CMOS Pass-Transistor Logic Dejan Markovic p. 36
- 2.1 Silicon on Insulator (SOI) Yuichi Kado p. 48
- 3 High-Speed, Low-Power Emitter Coupled Logic Circuits Tadahiro Kuroda p. 1
- 4 Price-Performance of Computer Technology John C. McCallum p. 1
- Section II Computer Systems and Architecture
- 5 Computer Architecture and Design Jean-Luc Gaudiot p. 1
- 5.1 Server Computer Architecture Siamack Haghighi p. 2
- 5.2 Very Large Instruction Word Architectures Binu Matthew p. 10
- 5.3 Vector Processing Krste Asanovic p. 22
- 5.4 Multithreading, Multiprocessing Manoj Franklin p. 32
- 5.5 Survey of Parallel Systems Donna Quammen p. 48
- 5.6 Virtual Memory Systems and TLB Structures Bruce Jacob p. 55
- 6 System Design
- 6.1 Superscalar Processors Mark Smotherman p. 1
- 6.2 Register Renaming Techniques Dezso Sima p. 6
- 6.3 Predicting Branches in Computer Programs Kevin Skadron p. 30
- 6.4 Network Processor Architecture Tzi-cker Chiueh p. 48
- 7 Architectures for Low Power Pradip Bose p. 1
- 8 Performance Evaluation
- 8.1 Measurement and Modeling of Disk Subsystem Performance Jozo J. Dujmovic and Daniel Tomasevich and Ming Au-Yeung p. 1
- 8.2 Performance Evaluation: Techniques, Tools, and Benchmarks Lizy Kurian John p. 20
- 8.3 Trace Caching and Trace Processors Eric Rotenberg p. 36
- 9 Computer Arithmetic
- 9.1 High-Speed Computer Arithmetic Earl E. Swartzlander, Jr. p. 1
- 9.2 Fast Adders and Multipliers Gensuke Goto p. 22
- Section III Design Techniques
- 10 Timing and Clocking
- 10.1 Design of High-Speed CMOS PLLs and DLLs John George Maneatis p. 1
- 10.2 Latches and Flip-Flops Fabian Klass p. 35
- 10.3 High-Performance Embedded SRAM Cyrus (Morteza) Afghahi p. 70
- 11 Multiple-Valued Logic Circuits K. Wayne Current p. 1
- 12 FPGAs for Rapid Prototyping James O. Hamblen p. 1
- 13 Issues in High-Frequency Processor Design Kevin J. Nowka p. 1
- Section IV Design for Low Power
- 14 Low-Power Design Issues Hemmige Varadarajan and Vivek Tiwari and Rakesh Patel and Hema Ramamurthy and Shahram Jamshidi and Snehal Jariwala and Wenjie Jiang p. 1
- 15 Low-Power Circuit Technologies Masayuki Miyazaki p. 1

- 16 Techniques for Leakage Power Reduction Vivek De and Ali Keshavarzi and Siva Narendra and Dinesh Somasekhar and Shekhar Borkar and James Kao and Raj Nair and Yibin Ye p. 1
- 17 Dynamic Voltage Scaling Thomas D. Burd p. 1
- 18 Low-Power Design of Systems on Chip Christian Piguet p. 1
- 19 Implementation-Level Impact on Low-Power Design Katsunori Seno p. 1
- 20 Accurate Power Estimation of Combinational CMOS Digital Circuits Hendrawan Soeleman and Kaushik Roy p. 1
- 21 Clock-Powered CMOS for Energy-Efficient Computing Nestoras Tzartzanis and William Athas p. 1
- Section V Embedded Applications
- 22 Embedded Systems-on-Chips Wayne Wolf p. 1
- 23 Embedded Processor Applications Jonathan W. Valvano p. 1
- Section VI Signal Processing
- 24 Digital Signal Processing Fred J. Taylor p. 1
- 25 DSP Applications Daniel Martin p. 1
- 26 Digital Filter Design Worayot Lertniphonphun and James H. McClellan p. 1
- 27 Audio Signal Processing Adam Dabrowski and Tomasz Marciniak p. 1
- 28 Digital Video Processing Todd R. Reed p. 1
- 29 Low-Power Digital Signal Processing Thucydides Xanthopoulos p. 1
- Section VII Communications and Networks
- 30 Communications and Computer Networks Anna Hac p. 1
- Section VIII Input/Output
- 31 Circuits for High-Performance I/O Chik-Kong Ken Yang p. 1
- 32 Algorithms and Data Structures in External Memory Jeffrey Scott Vitter p. 1
- 33 Parallel I/O Systems Peter J. Varman p. 1
- 34 A Read Channel for Magnetic Recording
- 34.1 Recording Physics and Organization of Data on a Disk Bane Vasic and Miroslav Despotovic p. 2
- 34.2 Read Channel Architecture Bane Vasic and Pervez M. Aziz and Necip Sayiner p. 10
- 34.3 Adaptive Equalization and Timing Recovery Pervez M. Aziz p. 19
- 34.4 Head Position Sensing in Disk Drives Ara Patapoutian p. 42
- 34.5 Modulation Codes for Storage Systems Brian Marcus and Emina Soljanin p. 51
- 34.6 Data Detection Miroslav Despotovic and Vojin Senk p. 62
- 34.7 An Introduction to Error-Correcting Codes Mario Blaum p. 87
- Section IX Operating System
- 35 Distributed Operating Systems Peter Reiher p. 1
- Section X New Directions in Computing
- 36 SPS: A Strategically Programmable System M. Sarrafzadeh and E. Bozorgzadeh and R. Kastner and S. O. Memik p. 1
- 37 Reconfigurable Processors
- 37.1 Reconfigurable Computing John Morris p. 1
- 37.2 Using Configurable Computing Systems Danny Newport and Don Bouldin p. 17
- 37.3 Xtensa: A Configurable and Extensible Processor Ricardo E. Gonzalez and Albert Wang p. 24

- 38 Roles of Software Technology in Intelligent Transportation Systems Shoichi Washino p. 1
- 39 Media Signal Processing
- 39.1 Instruction Set Architecture for Multimedia Signal Processing Ruby Lee p. 1
- 39.2 DSP Platform Architecture for SoC Products Gerald G. Pechanek p. 38
- 39.3 Digital Audio Processors for Personal Computer Systems Thomas C. Savell p. 47
- 39.4 Modern Approximation Iterative Algorithms and Their Applications in Computer Engineering Sadiq M. Sait and Habib Youssef p. 64
- 40 Internet Architectures Borko Furht p. 1
- 41 Microelectronics for Home Entertainment Yoshiaki Hagiwara p. 1
- 42 Mobile and Wireless Computing
- 42.1 Bluetooth--A Cable Replacement and More John F. Alexander and Raymond Barrett p. 2
- 42.2 Signal Processing ASIC Requirements for High-Speed Wireless Data Communications Babak Daneshrad p. 8
- 42.3 Communication System-on-a-Chip Samiha Mourad and Garret Okamoto p. 15
- 42.4 Communications and Computer Networks Mohammad Ilyas p. 26
- 42.5 Video over Mobile Networks Abdul H. Sadka p. 38
- 42.6 Pen-Based User Interfaces--An Applications Overview Giovanni Seni and Jayashree Subrahmonia p. 49
- 42.7 What Makes a Programmable DSP Processor Special? Ingrid Verbauwhede p. 64
- 43 Data Security Matt Franklin p. 1
- Section XI Testing and Design for Testability
- 44 System-on-Chip (SoC) Testing: Current Practices and Challenges for Tomorrow R. Chandramouli p. 1
- 45 Testing of Synchronous Sequential Digital Circuits U. Glaeser and Z. Stamenkovic and H. T. Vierhaus p. 1
- 46 Scan Testing Chouki Aktouf p. 1
- 47 Computer-Aided Analysis and Forecast of Integrated Circuit Yield Z. Stamenkovic and N. Stojadinovic p. 1
- Index p. 1