## Table of contents

- Preface (p. ix)
- 1 Computer Abstractions and Technology (p. 2)
- **1.1 Introduction** (p. 3)
- 1.2 Below Your Program (p. 11)
- **1.3 Under the Covers** (p. 15)
- 1.4 Real Stuff: Manufacturing Pentium 4 Chips (p. 28)
- 1.5 Fallacies and Pitfalls (p. 33)
- 1.6 Concluding Remarks (p. 35)
- 1.7 Historical Perspective and Further Reading (p. 36)
- **1.8 Exercises** (p. 36)
- Computers in the Real World: Information Technology for the 4 Billion without IT (p. 44)
- 2 Instructions: Language of the Computer (p. 46)
- **2.1 Introduction** (p. 48)
- 2.2 Operations of the Computer Hardware (p. 49)
- 2.3 Operands of the Computer Hardware (p. 52)
- 2.4 Representing Instructions in the Computer (p. 60)
- **2.5 Logical Operations** (p. 68)
- 2.6 Instructions for Making Decisions (p. 72)
- 2.7 Supporting Procedures in Computer Hardware (p. 79)
- 2.8 Communicating with People (p. 90)
- 2.9 MIPS Addressing for 32-Bit Immediates and Addresses (p. 95)
- **2.10 Translating and Starting a Program** (p. 106)
- 2.11 How Compilers Optimize (p. 116)
- 2.12 How Compilers Work: An Introduction (p. 121)
- 2.13 A C Sort Example to Put It All Together (p. 121)
- 2.14 Implementing an Object-Oriented Language (p. 130)
- **2.15 Arrays versus Pointers** (p. 130)
- **2.16 Real Stuff: IA-32 Instructions** (p. 134)
- **2.17 Fallacies and Pitfalls** (p. 143)
- 2.18 Concluding Remarks (p. 145)
- 2.19 Historical Perspective and Further Reading (p. 147)
- **2.20 Exercises** (p. 147)
- Computers in the Real World: Helping Save Our Environment with Data (p. 156)
- 3 Arithmetic for Computers (p. 158)
- **3.1 Introduction** (p. 160)
- 3.2 Signed and Unsigned Numbers (p. 160)
- 3.3 Addition and Subtraction (p. 170)
- **3.4 Multiplication** (p. 176)
- **3.5 Division** (p. 183)
- **3.6 Floating Point** (p. 189)
- 3.7 Real Stuff: Floating Point in the IA-32 (p. 217)
- 3.8 Fallacies and Pitfalls (p. 220)

- 3.9 Concluding Remarks (p. 225)
- 3.10 Historical Perspective and Further Reading (p. 229)
- **3.11 Exercises** (p. 229)
- Computers in the Real World: Reconstructing the Ancient World (p. 236)
- 4 Assessing and Understanding Performance (p. 238)
- **4.1 Introduction** (p. 240)
- **4.2 CPU Performance and Its Factors** (p. 246)
- **4.3 Evaluating Performance** (p. 254)
- 4.4 Real Stuff: Two SPEC Benchmarks and the Performance of Recent Intel Processors (p. 259)
- 4.5 Fallacies and Pitfalls (p. 266)
- 4.6 Concluding Remarks (p. 270)
- 4.7 Historical Perspective and Further Reading (p. 272)
- **4.8 Exercises** (p. 272)
- Computers in The Real World: Moving People Faster and More Safely (p. 280)
- 5 The Processor: Datapath and Control (p. 282)
- **5.1 Introduction** (p. 284)
- **5.2 Logic Design Conventions** (p. 289)
- 5.3 Building a Datapath (p. 292)
- **5.4 A Simple Implementation Scheme** (p. 300)
- 5.5 A Multicycle Implementation (p. 318)
- **5.6 Exceptions** (p. 340)
- 5.7 Microprogramming: Simplifying Control Design (p. 346)
- 5.8 An Introduction to Digital Design Using a Hardware Design Language (p. 346)
- 5.9 Real Stuff: The Organization of Recent Pentium Implementations (p. 347)
- **5.10 Fallacies and Pitfalls** (p. 350)
- **5.11 Concluding Remarks** (p. 352)
- 5.12 Historical Perspective and Further Reading (p. 353)
- **5.13 Exercises** (p. 354)
- Computers in the Real World: Empowering the Disabled (p. 366)
- 6 Enhancing Performance with Pipelining (p. 368)
- **6.1 An Overview of Pipelining** (p. 370)
- **6.2 A Pipelined Datapath** (p. 384)
- **6.3 Pipelined Control** (p. 399)
- **6.4 Data Hazards and Forwarding** (p. 402)
- **6.5 Data Hazards and Stalls** (p. 413)
- **6.6 Branch Hazards** (p. 416)
- 6.7 Using a Hardware Description Language to Describe and Model a Pipeline (p. 426)
- **6.8 Exceptions** (p. 427)
- 6.9 Advanced Pipelining: Extracting More Performance (p. 432)
- **6.10 Real Stuff: The Pentium 4 Pipeline** (p. 448)
- **6.11 Fallacies and Pitfalls** (p. 451)

- **6.12 Concluding Remarks** (p. 452)
- 6.13 Historical Perspective and Further Reading (p. 454)
- **6.14 Exercises** (p. 454)
- Computers in the Real World: Mass Communication without Gatekeepers (p. 464)
- 7 Large and Fast: Exploiting Memory Hierarchy (p. 466)
- **7.1 Introduction** (p. 468)
- **7.2 The Basics of Caches** (p. 473)
- 7.3 Measuring and Improving Cache Performance (p. 492)
- **7.4 Virtual Memory** (p. 511)
- 7.5 A Common Framework for Memory Hierarchies (p. 538)
- 7.6 Real Stuff: The Pentium P4 and the AMD Opteron Memory Hierarchies (p. 546)
- 7.7 Fallacies and Pitfalls (p. 550)
- **7.8 Concluding Remarks** (p. 552)
- 7.9 Historical Perspective and Further Reading (p. 555)
- **7.10 Exercises** (p. 555)
- Computers in the Real World: Saving the World's Art Treasures (p. 562)
- 8 Storage, Networks, and Other Peripherals (p. 564)
- **8.1 Introduction** (p. 566)
- 8.2 Disk Storage and Dependability (p. 569)
- **8.3 Networks** (p. 580)
- 8.4 Buses and Other Connections between Processors, Memory, and I/O Devices (p. 581)
- 8.5 Interfacing I/O Devices to the Processor, Memory, and Operating System (p. 588)
- 8.6 I/O Performance Measures: Examples from Disk and File Systems (p. 597)
- **8.7 Designing an I/O System** (p. 600)
- 8.8 Real Stuff: A Digital Camera (p. 603)
- **8.9 Fallacies and Pitfalls** (p. 606)
- **8.10 Concluding Remarks** (p. 609)
- 8.11 Historical Perspective and Further Reading (p. 611)
- **8.12 Exercises** (p. 611)
- Computers in the Real World: Saving Lives through Better Diagnosis (p. 622)
- 9 Multiprocessors and Clusters (p. 2)
- **9.1 Introduction** (p. 4)
- 9.2 Programming Multiprocessors (p. 8)
- 9.3 Multiprocessors Connected by a Single Bus (p. 11)
- 9.4 Multiprocessors Connected by a Network (p. 20)
- **9.5 Clusters** (p. 25)
- 9.6 Network Topologies (p. 27)
- 9.7 Multiprocessors Inside a Chip and Multithreading (p. 30)
- 9.8 Real Stuff: The Google Cluster of PCs (p. 34)
- **9.9 Fallacies and Pitfalls** (p. 39)

- 9.10 Concluding Remarks (p. 42)
- 9.11 Historical Perspective and Further Reading (p. 47)
- **9.12 Exercises** (p. 55)
- Appendices
- A Assemblers, Linkers, and the SPIM Simulator (p. 2)
- **A.1 Introduction** (p. 3)
- **A.2 Assemblers** (p. 10)
- **A.3 Linkers** (p. 18)
- **A.4 Loading** (p. 19)
- **A.5 Memory Usage** (p. 20)
- A.6 Procedure Call Convention (p. 22)
- A.7 Exceptions and Interrupts (p. 33)
- **A.8 Input and Output** (p. 38)
- **A.9 SPIM** (p. 40)
- A.10 MIPS R2000 Assembly Language (p. 45)
- A.11 Concluding Remarks (p. 81)
- **A.12 Exercises** (p. 82)
- B The Basics of Logic Design (p. 2)
- **B.1 Introduction** (p. 3)
- B.2 Gates, Truth Tables, and Logic Equations (p. 4)
- **B.3 Combinational Logic** (p. 8)
- **B.4 Using a Hardware Description Language** (p. 20)
- B.5 Constructing a Basic Arithmetic Logic Unit (p. 26)
- **B.6 Faster Addition: Carry Lookahead** (p. 38)
- **B.7 Clocks** (p. 47)
- B.8 Memory Elements: Flip-flops, Latches, and Registers (p. 49)
- **B.9 Memory Elements: SRAMs and DRAMs** (p. 57)
- B.10 Finite State Machines (p. 67)
- **B.11 Timing Methodologies** (p. 72)
- **B.12 Field Programmable Devices** (p. 77)
- **B.13 Concluding Remarks** (p. 78)
- **B.14 Exercises** (p. 79)
- C Mapping Control to Hardware (p. 2)
- **C.1 Introduction** (p. 3)
- C.2 Implementing Combinational Control Units (p. 4)
- C.3 Implementing Finite State Machine Control (p. 8)
- C.4 Implementing the Next-State Function with a Sequencer (p. 21)
- C.5 Translating a Microprogram to Hardware (p. 27)
- C.6 Concluding Remarks (p. 31)
- **C.7 Exercises** (p. 32)
- D A Survey of RISC Architectures for Desktop, Server, and Embedded Computers (p. 2)
- **D.1 Introduction** (p. 3)
- D.2 Addressing Modes and Instruction Formats (p. 5)
- D.3 Instructions: The MIPS Core Subset (p. 9)

- D.4 Instructions: Multimedia Extensions of the Desktop/Server RISCs (p. 16)
- D.5 Instructions: Digital Signal-Processing Extensions of the Embedded RISCs (p. 19)
- D.6 Instructions: Common Extensions to MIPS Core (p. 20)
- **D.7 Instructions Unique to MIPS64** (p. 25)
- D.8 Instructions Unique to Alpha (p. 27)
- **D.9 Instructions Unique to SPARC v.9** (p. 29)
- **D.10 Instructions Unique to PowerPC** (p. 32)
- **D.11 Instructions Unique to PA-RISC 2.0** (p. 34)
- **D.12 Instructions Unique to ARM** (p. 36)
- **D.13 Instructions Unique to Thumb** (p. 38)
- **D.14 Instructions Unique to SuperH** (p. 39)
- **D.15 Instructions Unique to M32R** (p. 40)
- **D.16 Instructions Unique to MIPS16** (p. 41)
- **D.17 Concluding Remarks** (p. 43)
- **D.18 Acknowledgments** (p. 46)
- **D.19 References** (p. 47)
- **Index** (p. 1)
- **Glossary** (p. 1)
- Further Reading (p. 1)