

- 1 An Introduction to Memory Chip Design p. 1
- 1.1 Introduction p. 1
- 1.2 The Internal Organization of Memory Chips p. 3
 - 1.2.1 The Memory Cell Array p. 3
 - 1.2.2 The Peripheral Circuit p. 5
 - 1.2.3 The I/O Interface Circuit p. 6
- 1.3 Categories of Memory Chip p. 6
- 1.4 General Trends in DRAM Design and Technology p. 11
 - 1.4.1 The History of Memory-Cell Development p. 11
 - 1.4.2 The Basic Operation of The 1-T Cell p. 15
 - 1.4.3 Advances in DRAM Design and Technology p. 19
- 1.5 General Trends in SRAM Design and Technology p. 24
 - 1.5.1 The History of Memory-Cell Development p. 24
 - 1.5.2 The Basic Operation of a SRAM Cell p. 26
 - 1.5.3 Advances in SRAM Design and Technology p. 29
- 1.6 General Trends in Non-Volatile Memory Design and Technology p. 31
 - 1.6.1 The History of Memory-Cell Development p. 31
 - 1.6.2 The Basic Operation of Flash Memory Cells p. 34
 - 1.6.3 Advances in Flash-Memory Design and Technology p. 46
- 2 The Basics of RAM Design and Technology p. 49
 - 2.1 Introduction p. 49
 - 2.2 Devices p. 49
 - 2.2.1 MOSFETs p. 49
 - 2.2.2 Capacitors p. 57
 - 2.2.3 Resistors p. 60
 - 2.2.4 Wiring and Wiring Materials p. 61
 - 2.2.5 Silicon Substrates and CMOS Latch-Up p. 65
 - 2.2.6 Other Devices p. 67
 - 2.3 NMOS Static Circuits p. 67
 - 2.3.1 The dc Characteristics of an Inverter p. 68
 - 2.3.2 The ac Characteristics of an Inverter p. 70
 - 2.3.3 The Improved NMOS Static Inverter p. 74
 - 2.4 NMOS Dynamic Circuits p. 76
 - 2.4.1 The Dynamic Inverter p. 76
 - 2.4.2 The Bootstrap Driver p. 77
 - 2.5 CMOS Circuits p. 79
 - 2.5.1 The dc Characteristics p. 80
 - 2.5.2 The ac Characteristics p. 82
 - 2.6 Basic Memory Circuits p. 83
 - 2.6.1 The Inverter and the Basic Logic Gate p. 83
 - 2.6.2 The Current Mirror p. 83
 - 2.6.3 The Differential Amplifier p. 83
 - 2.6.4 The Voltage Booster p. 87
 - 2.6.5 The Level Shifter p. 88
 - 2.6.6 The Ring Oscillator p. 88
 - 2.6.7 The Counter p. 89

- 2.7 The Scaling Law p. 90
- 2.7.1 Constant Electric-Field Scaling p. 90
- 2.7.2 Constant Operation-Voltage Scaling p. 92
- 2.7.3 Combined Scaling p. 92
- 2.8 Lithography p. 93
- 2.9 Packaging p. 94
- 3 DRAM Circuits p. 97
- 3.1 Introduction p. 97
- 3.1.1 High-Density Technology p. 98
- 3.1.2 High-Performance Circuits p. 100
- 3.2 The catalog Specifications of the Standard DRAM p. 102
- 3.2.1 Operational Conditions p. 102
- 3.2.2 Modes of Operation and Timing Specifications p. 105
- 3.3 The Basic Configuration and Operation of the DRAM Chip p. 110
- 3.3.1 Chip Configuration p. 110
- 3.3.2 Address Multiplexing p. 111
- 3.4 Fundamental Chip Technologies p. 113
- 3.4.1 A Larger Memory Capacity and Scaled-Down Devices p. 113
- 3.4.2 High S/N Ratio Circuits p. 116
- 3.4.3 Low Power Circuits p. 117
- 3.4.4 High-Speed Circuits p. 123
- 3.4.5 The Multidivision of a Memory Array p. 128
- 3.5 The Multidivided Data Line and Word Line p. 131
- 3.5.1 The Multidivided Data Line p. 132
- 3.5.2 The Multidivided Word Line p. 139
- 3.6 Read and Relevant Circuits p. 141
- 3.6.1 The Address Buffer p. 141
- 3.6.2 The Address Decoder p. 144
- 3.6.3 The Word Driver p. 147
- 3.6.4 The Sensing Circuit p. 157
- 3.6.5 The Common I/O-Line Relevant Circuit p. 167
- 3.6.6 The Data-Output Buffer p. 172
- 3.7 Write and Relevant Circuits p. 174
- 3.8 Refresh-Relevant Circuits p. 175
- 3.8.1 Refresh Schemes p. 175
- 3.8.2 The Extension of Data-Retention Time in Active Mode p. 176
- 3.8.3 Current Reduction Circuits in Data-Retention Mode p. 176
- 3.9 Redundancy Techniques p. 178
- 3.9.1 Issues for Large-Memory-Capacity Chips p. 184
- 3.9.2 Intra-Subarray Replacement Redundancy p. 185
- 3.9.3 Inter-Subarray Replacement Redundancy p. 189
- 3.9.4 The Repair of dc-Characteristics Faults p. 191
- 3.10 On-Chip Testing Circuits p. 192
- 4 High Signal-to-Noise Ratio DRAM Design and Technology p. 195
- 4.1 Introduction p. 195
- 4.2 Trends in High S/N Ratio Design p. 195

- 4.2.1 The Signal Charge p. 197
- 4.2.2 Leakage Charge p. 204
- 4.2.3 The Soft-Error Critical Charge p. 208
- 4.2.4 The Data-Line Noise Charge p. 210
- 4.3 Data-Line Noise Reduction p. 210
 - 4.3.1 Noise Sources and Their Reduction p. 210
 - 4.3.2 Word-Line Drive Noise p. 213
 - 4.3.3 Data-Line and Sense-Amplifier Imbalances p. 217
 - 4.3.4 Word-Line to Data-Line Coupling Noise p. 230
 - 4.3.5 Data-Line Interference Noise p. 237
 - 4.3.6 Power-Supply Voltage Bounce p. 240
 - 4.3.7 Variation in the Reference Voltage p. 241
 - 4.3.8 Other Noises p. 244
- 4.4 Summary p. 247
- 5 On-Chip Voltage Generators p. 249
 - 5.1 Introduction p. 249
 - 5.2 The Substrate-Bias Voltage (V_{BB}) Generator p. 251
 - 5.2.1 The Roles of the V_{BB} generator p. 251
 - 5.2.2 Basic Operation and Design Issues p. 256
 - 5.2.3 Power-On Characteristics p. 258
 - 5.2.4 Characteristics in the High- V_{DD} Region p. 264
 - 5.2.5 The V_{BB} Bump p. 266
 - 5.2.6 Substrate-Current Generation p. 269
 - 5.2.7 Triple-Well Structures p. 272
 - 5.2.8 Low-Power V_{BB} Generators p. 273
 - 5.3 The Voltage Up-Converter p. 276
 - 5.3.1 The Roles of the Voltage Up-Converter p. 276
 - 5.3.2 Design Approaches and Issues p. 278
 - 5.3.3 High Boost-Ratio Converters p. 283
 - 5.3.4 Low-Power, High Supply Current Converters p. 285
 - 5.4 The Voltage Down-Converter p. 290
 - 5.4.1 The Roles of the Voltage Down-Converter p. 290
 - 5.4.2 The Negative-Feedback Converter and Design Issues p. 293
 - 5.4.3 Optimum Design p. 297
 - 5.4.4 Phase Compensation p. 301
 - 5.4.5 Reference-Voltage Generators p. 316
 - 5.4.6 Burn-In Test Circuits p. 323
 - 5.4.7 Voltage Trimming p. 327
 - 5.4.8 Low-Power Circuits p. 329
 - 5.5 The Half- V_{DD} Generator p. 332
 - 5.6 Examples of Advanced On-Chip Voltage Generators p. 333
- 6 High-Performance Subsystem Memories p. 339
 - 6.1 Introduction p. 339
 - 6.2 Hierarchical Memory Systems p. 341
 - 6.2.1 Memory Hierarchy p. 341
 - 6.2.2 Improvements in Memory-Subsystem Performance p. 344

- 6.2.3 Memory-Chip Performance p. 349
- 6.3 Memory-Subsystem Technologies p. 354
- 6.3.1 Wide-Bit I/O Chip Configurations p. 354
- 6.3.2 Parallel Operation of Multidivided Arrays p. 354
- 6.3.3 Multibank Interleaving p. 357
- 6.3.4 Synchronous Operation p. 358
- 6.3.5 Pipeline/Prefetch Operations p. 362
- 6.3.6 High-Speed Clocking Schemes p. 363
- 6.3.7 Terminated I/O Interfaces p. 363
- 6.3.8 High-Density Packaging p. 364
- 6.4 High-Performance Standard DRAMs p. 365
- 6.4.1 Trends in Chip Development p. 365
- 6.4.2 Synchronous DRAM p. 368
- 6.4.3 Rambus DRAM p. 380
- 6.5 Embedded Memories p. 383
- 7 Low-Power Memory Circuits p. 389
- 7.1 Introduction p. 389
- 7.2 Sources and Reduction of Power Dissipation in a RAM Subsystem p. 392
- 7.2.1 Wide-Bit I/O Chip Configuration p. 393
- 7.2.2 Small Package p. 394
- 7.2.3 The Low-Voltage Data-Bus Interface p. 396
- 7.3 Sources of Power Dissipation in the RAM Chip p. 402
- 7.3.1 Active Power Sources p. 402
- 7.3.2 Data-Retention Power Sources p. 405
- 7.4 Low-Power DRAM Circuits p. 406
- 7.4.1 Active Power Reduction p. 406
- 7.4.2 Data-Retention Power Reduction p. 412
- 7.5 Low-Power SRAM Circuits p. 413
- 7.5.1 Active Power Reduction p. 413
- 7.5.2 Data-Retention Power Reduction p. 423
- 8 Ultra-Low-Voltage Memory Circuits p. 425
- 8.1 Introduction p. 425
- 8.2 Design Issues for Ultra-Low-Voltage RAM Circuits p. 426
- 8.2.1 Reduction of the Subthreshold Current p. 426
- 8.2.2 Stable Memory-Cell Operation p. 432
- 8.2.3 Suppression of, or Compensation for, Design Parameter Variations p. 433
- 8.2.4 Power-Supply Standardization p. 435
- 8.3 Ultra-Low-Voltage DRAM Circuits p. 437
- 8.3.1 Gate Boosting Circuit p. 439
- 8.3.2 The Multi- V_T Circuit p. 440
- 8.3.3 The Gate-Source Back-Biasing Circuit p. 442
- 8.3.4 The Well Control Circuit p. 456
- 8.3.5 The Source Control Circuit p. 461
- 8.3.6 The Well and Source Control Circuit p. 462
- 8.4 Ultra-Low-Voltage SRAM Circuits p. 463
- 8.5 Ultra-Low-Voltage SOI Circuits p. 466

- References p. 473
- Index p. 489