Introduction:

Soft Error Modeling –

Soft Error Rate Estimation of VLSI circuits –

Process Variation Aware Soft Error Rate Estimation Method for Integrated Circuits –

GPU-Accelerated Soft Error Rate Analysis of Large-scale Integrated Circuits –

FPGA Hardware Acceleration of Soft Error Rate Estimation of Digital Circuits –

Soft Error Tolerant Circuit Design using Partitioning-based Gate Sizing –

Resynthesize Technique for Soft Error Tolerant Design of Combinational Circuits